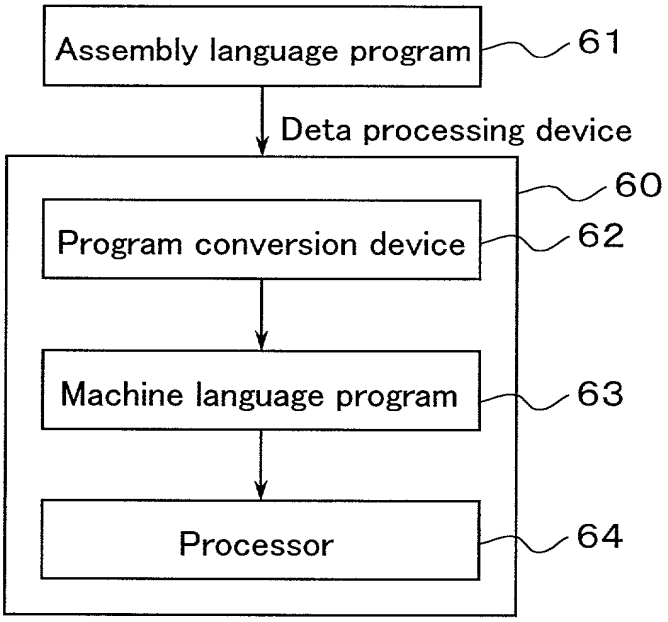
Assembly language program
61
Deta processing device
60
Program conversion device
62
Machine language program
63
Processor
64

FIG. 1

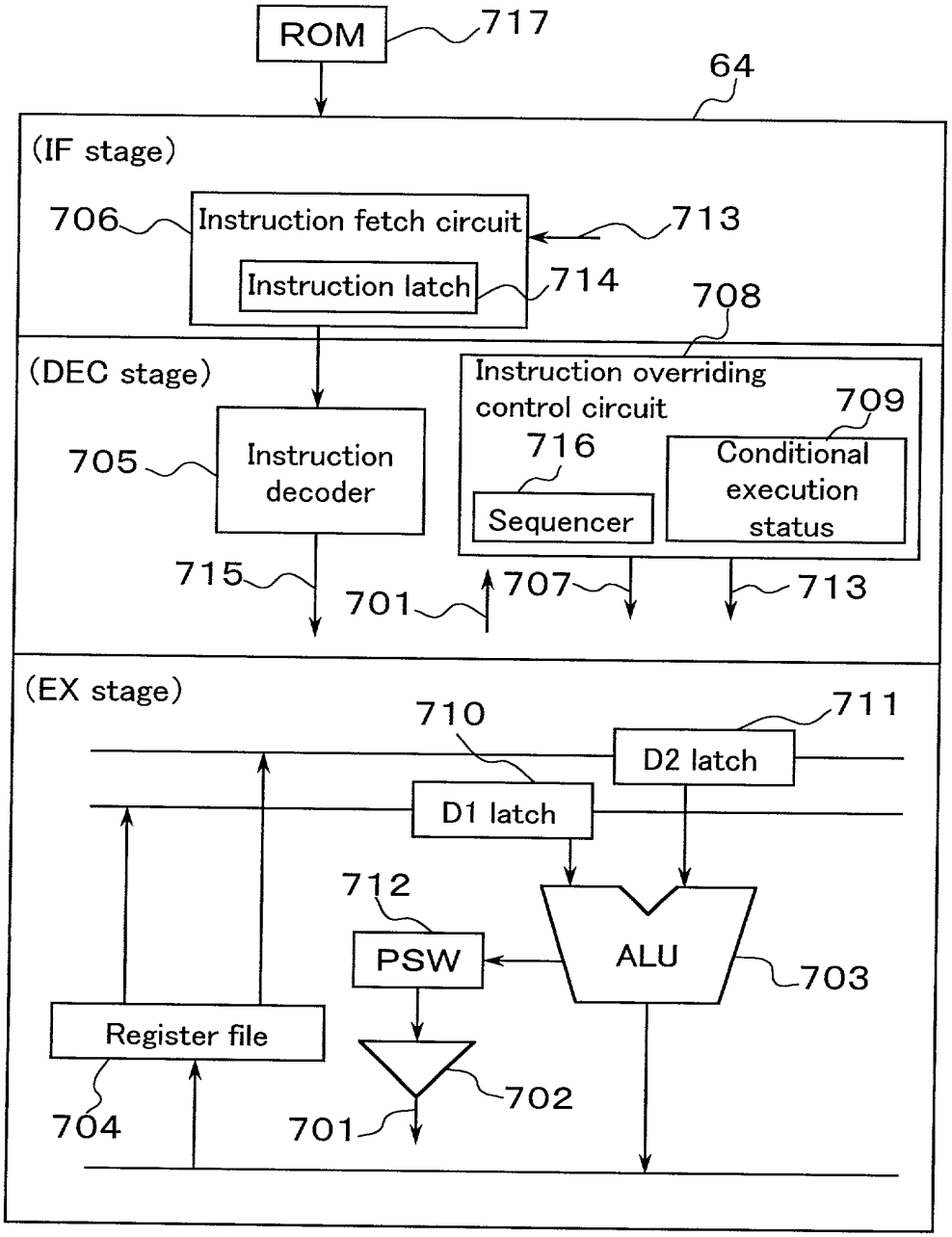
ROM
717
64
(IF stage)
706
Instruction fetch circuit
713
Instruction latch
714
708
(DEC stage)
Instruction overriding control circuit
709
705
Instruction decoder
716
Conditional execution status
Sequencer
715
701
707
713
(EX stage)
710
711
D2 latch
D1 latch
712
PSW
ALU
703
Register file
702
704
701

FIG. 2

Conditional execution status / Exclusive condition	x'00	x'01	x'10	x'11
1	Instruction overriding signal "0"	Instruction overriding signal "1"	Instruction overriding signal "0"	Instruction overriding signal "0"
0	Instruction overriding signal "0"	Instruction overriding signal "0"	Instruction overriding signal "1"	Instruction overriding signal "0"

FIG. 3A

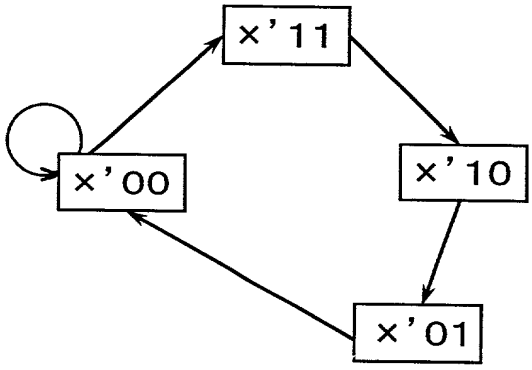

FIG. 3B

IF stage	Instruction 1	Instruction 2	Instruction 3	Instruction 4	Instruction 5	Instruction 6
DEC stage		Instruction 1	Instruction 2	Instruction 3	Instruction 4	Instruction 5
EX stage			Instruction 1	Instruction 2		Instruction 4

Conditional execution status	x'00	x'00	x'11	x'10	x'01	x'00	x'00
Exclusive condition	0	0	0	1	1	1	0
Instruction overriding signal	0	0	0	0	1	0	0
	t1	t2	t3	t4	t5	t6	
	[t11 t12]	[t21 t22]	[t31 t32]	[t41 t42]	[t51 t52]	[t61 t62]	

FIG. 4

First line	SUBIFEZF R0,R1
Second line	MOV R2,R4
Third line	MOV R3,R4
Fourth line	ADD R5,R6
Fifth line	NOP
Sixth line	NOP

FIG. 5

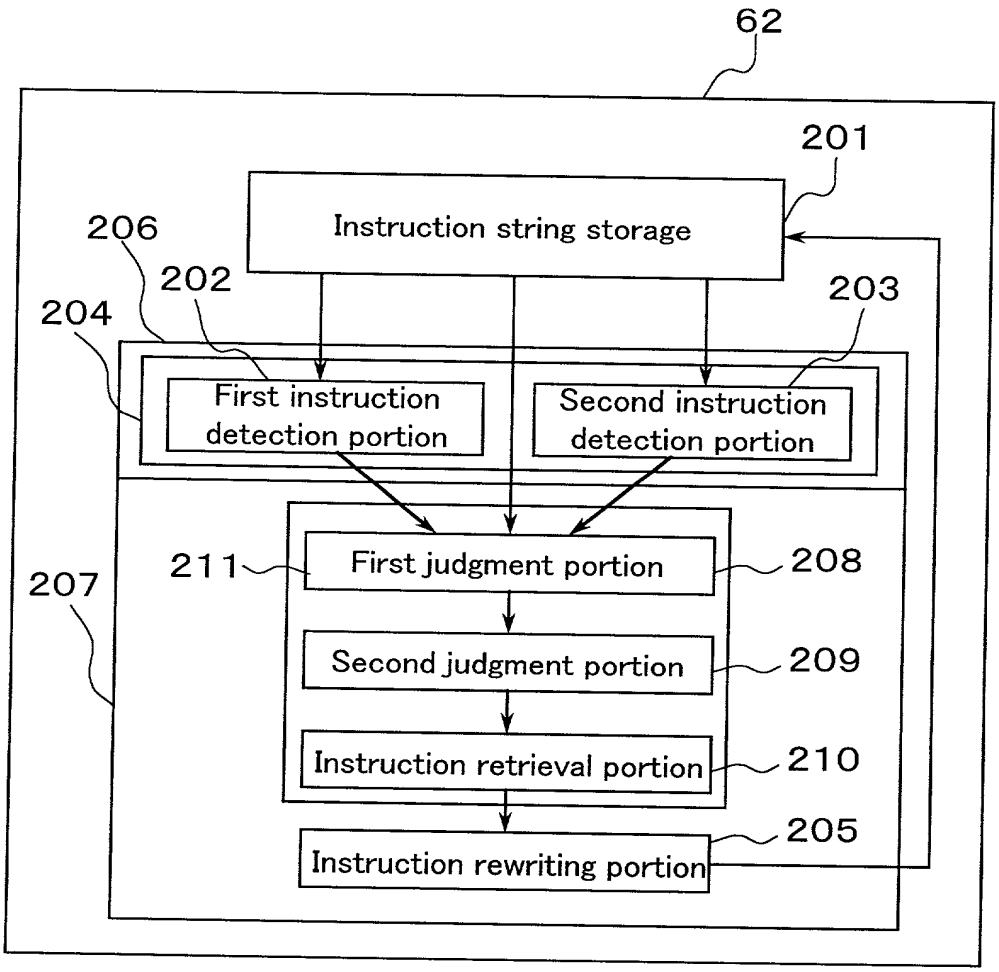
62
201
Instruction string storage
206
202
204
203
First instruction detection portion
Second instruction detection portion
211
First judgment portion
208
207
Second judgment portion
209
Instruction retrieval portion
210
205
Instruction rewriting portion

FIG. 6

First line	ADD R5,R1
Second line	SUB R0,R1
Third line	MOVIFZF R2,R4
Fourth line	MOVIFNZF R3,R4
Fifth line	ADD R4,R5
Sixth line	MOV R5,R7
Seventh line	MOVIFZF x'0001,R6
Eighth line	MOV R6,R0

FIG. 7

First line	ADD R5,R1
Second line	SUBIFEZF R0,R1
Third line	MOV R2,R4
Fourth line	MOV R3,R4
Fifth line	ADD R4,R5
Sixth line	MOV R5,R7
Seventh line	MOVIFZF x'0001,R6
Eighth line	MOV R6,R0

FIG. 8

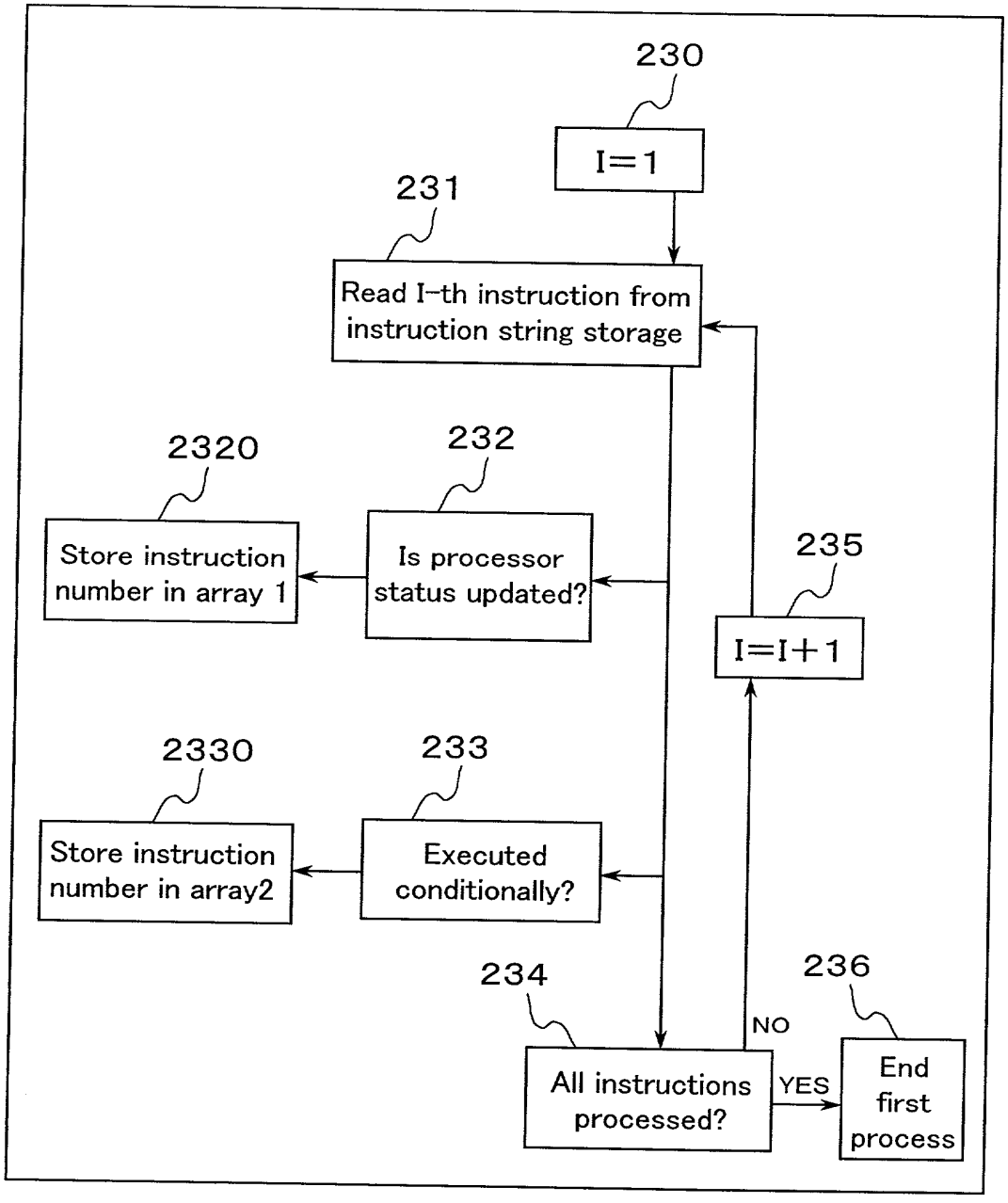
230
I=1
231
Read I-th instruction from instruction string storage
2320
232
Store instruction number in array 1
Is processor status updated?
235
I=I+1
2330
233
Store instruction number in array2
Executed conditionally?
234
236
NO
All instructions processed?
YES
End first process

FIG. 9

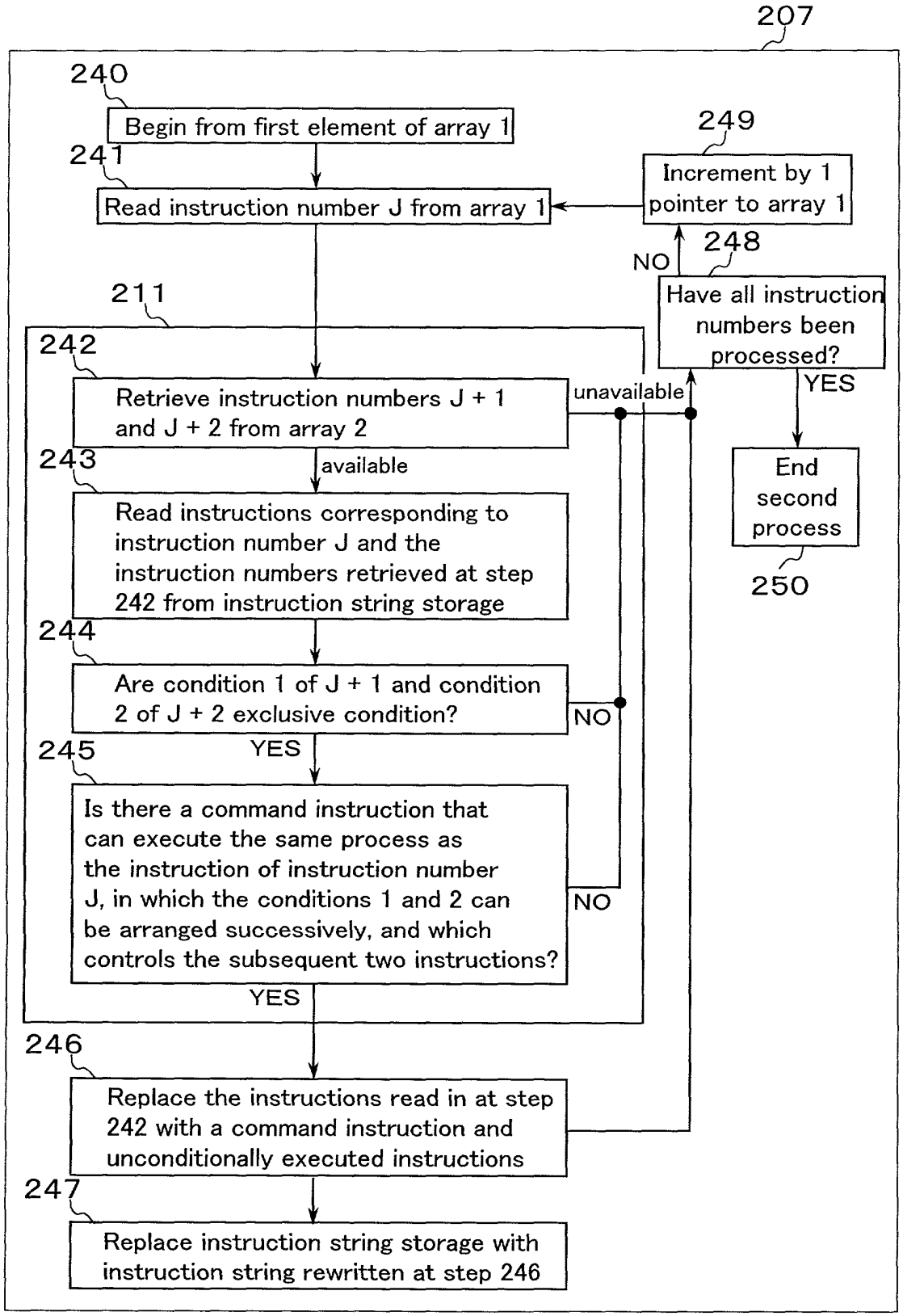
207
240
Begin from first element of array 1
241
Read instruction number J from array 1
249
Increment by 1 pointer to array 1
248
NO
Have all instruction numbers been processed?
YES
End second process
250
211
242
Retrieve instruction numbers J + 1 and J + 2 from array 2
unavailable
243
available
Read instructions corresponding to instruction number J and the instruction numbers retrieved at step 242 from instruction string storage
244
Are condition 1 of J + 1 and condition 2 of J + 2 exclusive condition?
NO
245
YES
Is there a command instruction that can execute the same process as the instruction of instruction number J, in which the conditions 1 and 2 can be arranged successively, and which controls the subsequent two instructions?
NO
YES
246
Replace the instructions read in at step 242 with a command instruction and unconditionally executed instructions
247
Replace instruction string storage with instruction string rewritten at step 246

FIG. 10

Conditional execution status / Exclusive condition	x'000	x'010 or x'001	x'100 or x'011	x'101
1	Instruction overriding signal "0"	Instruction overriding signal "1"	Instruction overriding signal "0"	Instruction overriding signal "0"
0	Instruction overriding signal "0"	Instruction overriding signal "0"	Instruction overriding signal "1"	Instruction overriding signal "0"

FIG. 11A

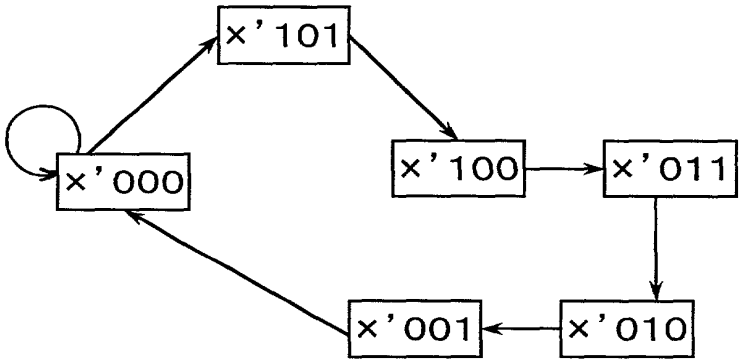

FIG. 11B

First line	SUBIFEXZF R0,R1
Second line	MOV R2,R6
Third line	MOV R3,R7
Fourth line	MOV R4,R6
Fifth line	MOV R5,R7
Sixth line	MOV x'0001,R6
Seventh line	ADD R0,R6
Eighth line	NOP

FIG. 12

IF stage	Instruction 1	Instruction 2	Instruction 3	Instruction 4	Instruction 5	Instruction 6	Instruction 7	Instruction 8
DEC stage		Instruction 1	Instruction 2	Instruction 3	Instruction 4	Instruction 5	Instruction 6	Instruction 7
EX stage			Instruction 1	Instruction 2	Instruction 3			Instruction 6

Conditional execution status	x'000	x'000	x'101	x'100	x'011	x'010	x'001	x'000	x'000
Exclusive condition	0	0	0	1	1	1	1	1	1
Instruction overriding signal	0	0	0	0	0	1	1	0	0
	t1	t2	t3	t4	t5	t6	t7	t8	
	[t11 t12]	[t21 t22]	[t31 t32]	[t41 t42]	[t51 t52]	[t61 t62]	[t71 t72]	[t81 t82]	

FIG. 13

First line	SUB R0,R1
Second line	MOVIFZF R2,R6
Third line	MOVIFZF R3,R7
Fourth line	MOVIFNZF R4,R6
Fifth line	MOVIFNZF R5,R7
Sixth line	MOV x'0001,R6
Seventh line	ADD R0,R6
Eighth line	NOP

FIG. 14

First line	SUB R0,R1
Second line	MOVIFZF R2,R6
Third line	MOVIFNZF R4,R6
Fourth line	MOVIFNZF R5,R7
Fifth line	MOVIFZF R3,R7
Sixth line	MOV x'0001,R6
Seventh line	ADD R0,R6
Eighth line	NOP

FIG. 15

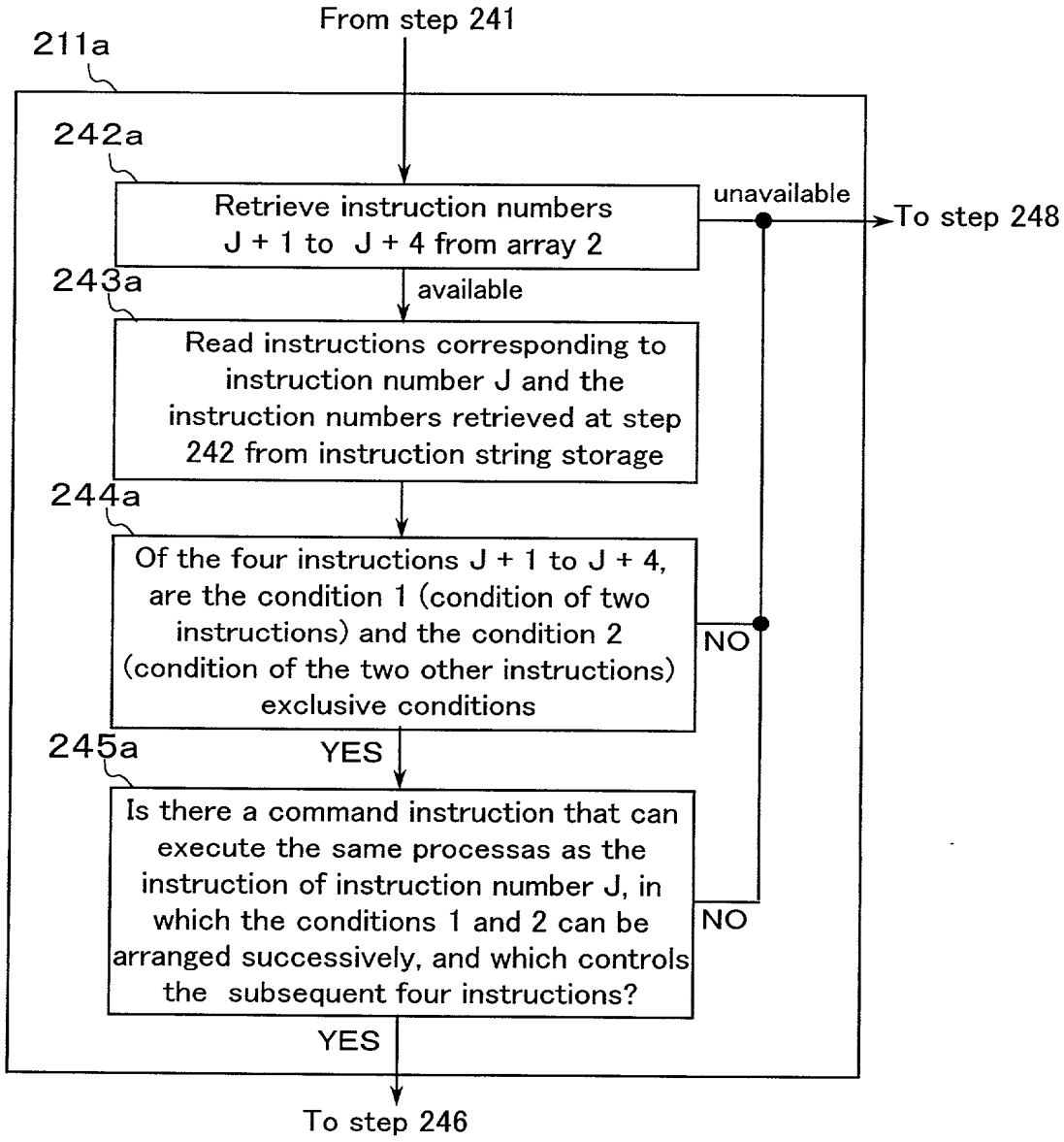
From step 241
211a
242a
Retrieve instruction numbers J + 1 to J + 4 from array 2
unavailable
To step 248
243a
available
Read instructions corresponding to instruction number J and the instruction numbers retrieved at step 242 from instruction string storage
244a
Of the four instructions J + 1 to J + 4, are the condition 1 (condition of two instructions) and the condition 2 (condition of the two other instructions) exclusive conditions
NO
245a
YES
Is there a command instruction that can execute the same processas as the instruction of instruction number J, in which the conditions 1 and 2 can be arranged successively, and which controls the subsequent four instructions?
NO
YES
To step 246

FIG. 16

Conditional execution status / Exclusive condition	x'00	x'01	x'10
1	Instruction overriding signal "0"	Instruction overriding signal "1"	Instruction overriding signal "0"
0	Instruction overriding signal "0"	Instruction overriding signal "0"	Instruction overriding signal "0"

FIG. 17A

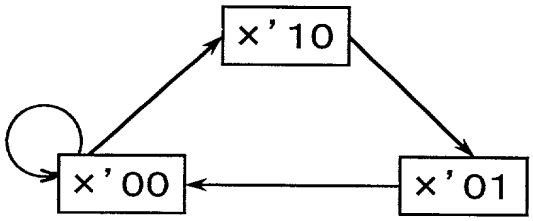

FIG. 17B

First line	SUBIFXZF R0,R1
Second line	MOV R2,R3
Third line	ADD R3,R6
Fourth line	MOV R4,R7

FIG. 18

IF stage	Instruction 1	Instruction 2	Instruction 3	Instruction 4	Instruction 5
DEC stage		Instruction 1	Instruction 2	Instruction 3	Instruction 4
EX stage			Instruction 1	X	Instruction 3

Conditional execution status	x'00	x'00	x'10	x'01	x'00	x'00
Exclusive condition	0	0	0	1	1	1
Instruction overriding signal	0	0	0	1	0	0
	t1 [t11 t12]	t2 [t21 t22]	t3 [t31 t32]	t4 [t41 t42]	t5 [t51 t52]	

FIG. 19

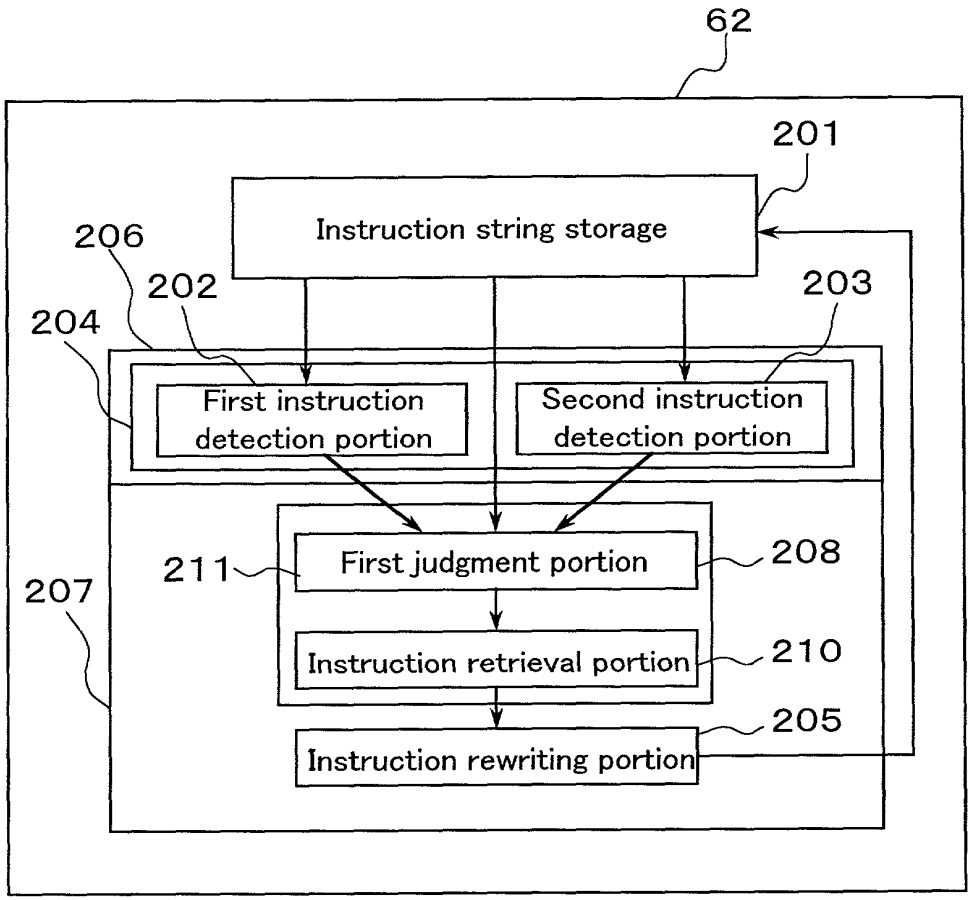
62
201
Instruction string storage
206
202
203
204
First instruction detection portion
Second instruction detection portion
211
First judgment portion
208
207
Instruction retrieval portion
210
205
Instruction rewriting portion

FIG. 20

First line	SUB R0,R1
Second line	MOVIFNZF R2,R3
Third line	ADD R3,R6
Fourth line	MOV R4,R7

FIG. 21

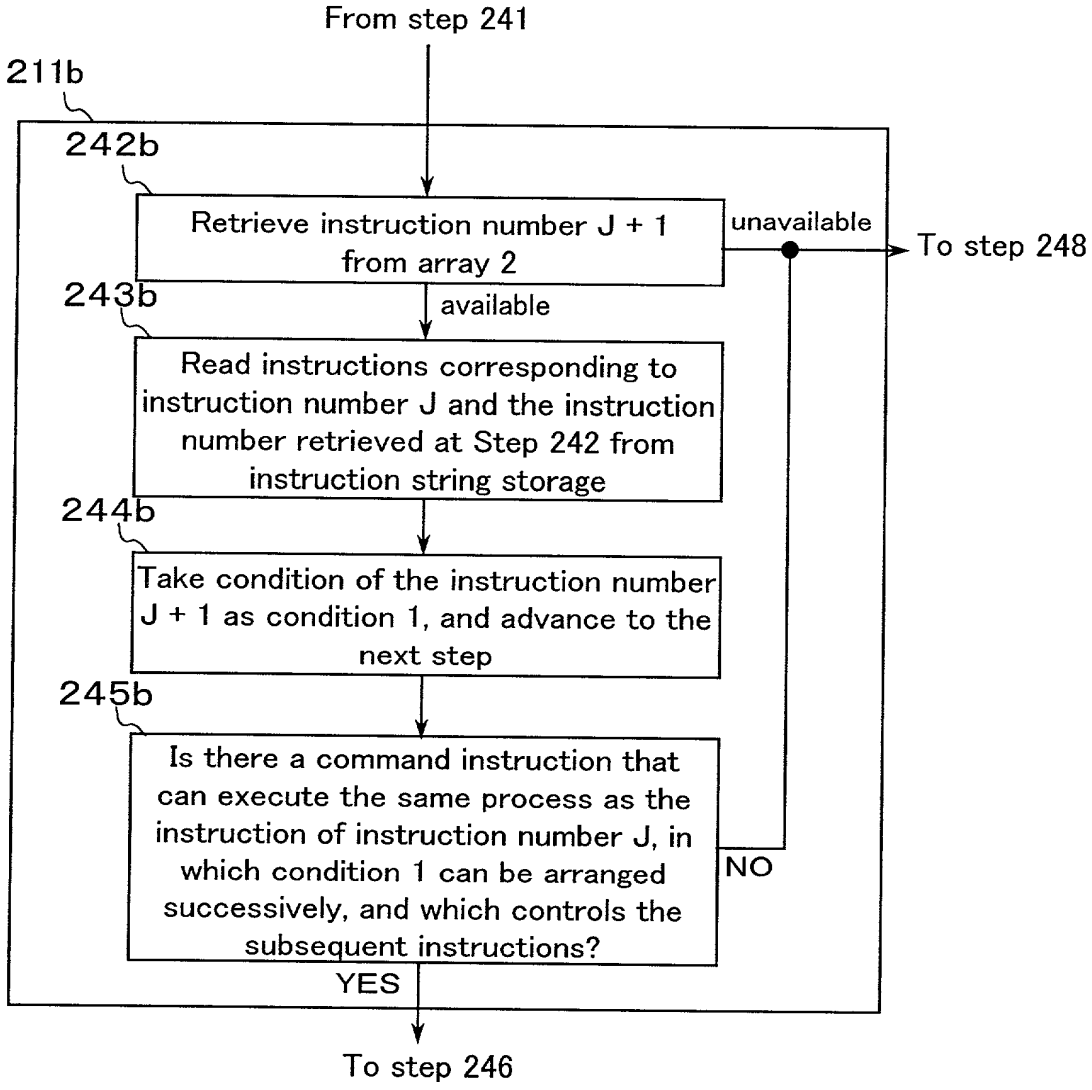
From step 241
211b
242b
Retrieve instruction number J + 1 from array 2
unavailable
To step 248
243b
available
Read instructions corresponding to instruction number J and the instruction number retrieved at Step 242 from instruction string storage
244b
Take condition of the instruction number J + 1 as condition 1, and advance to the next step
245b
Is there a command instruction that can execute the same process as the instruction of instruction number J, in which condition 1 can be arranged successively, and which controls the subsequent instructions?
NO
YES
To step 246

FIG. 22

Conditional execution status / Exclusive condition	×'00	×'01	×'10	×'11
1	Instruction overriding signal "0"	Instruction overriding signal "1"	Instruction overriding signal "1"	Instruction overriding signal "0"
0	Instruction overriding signal "0"	Instruction overriding signal "0"	Instruction overriding signal "0"	Instruction overriding signal "0"

FIG. 23A

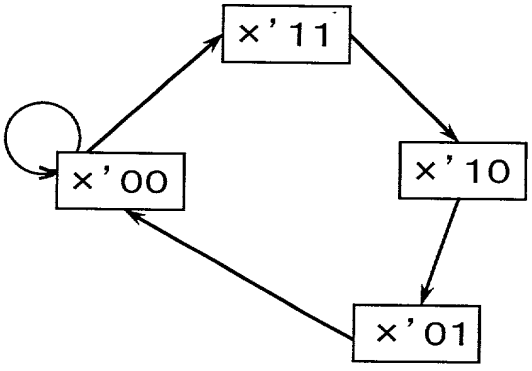

FIG. 23B

First line	SUBIFNXZF R0,R1
Second line	MOV R2,R3
Third line	MOV R5,R4
Fourth line	ADD R3,R6
Fifth LINE	MOV R4,R7

FIG. 24

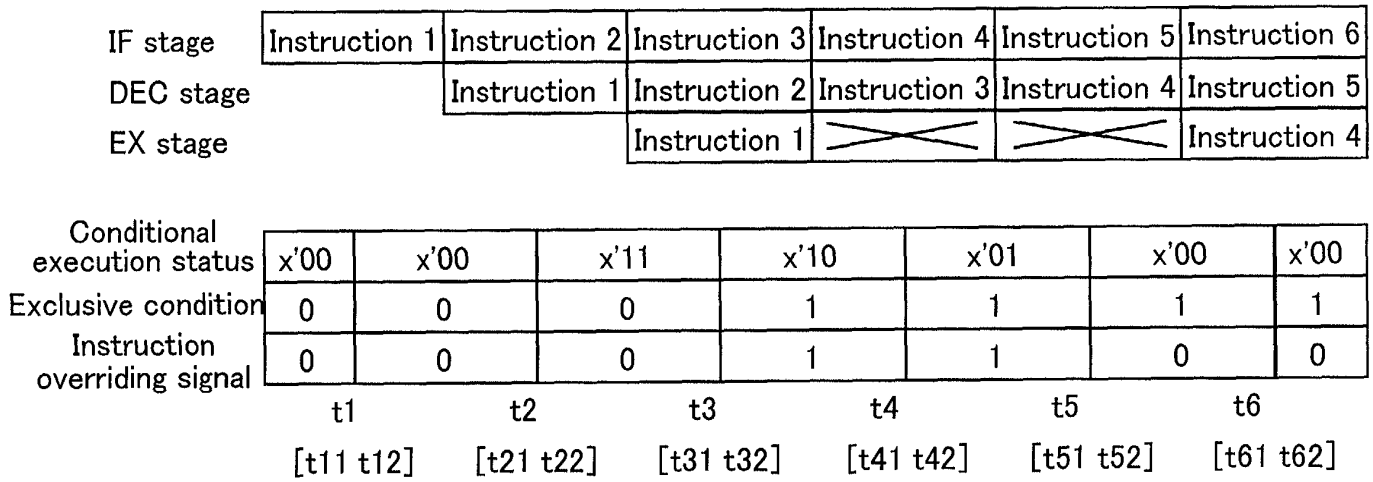

FIG. 25

First line	SUB R0,R1
Second line	MOVIFNZF R2,R3
Third line	MOVIFNZF R5,R4
Fourth line	ADD R3,R6
Fifth line	MOV R4,R7

FIG. 26

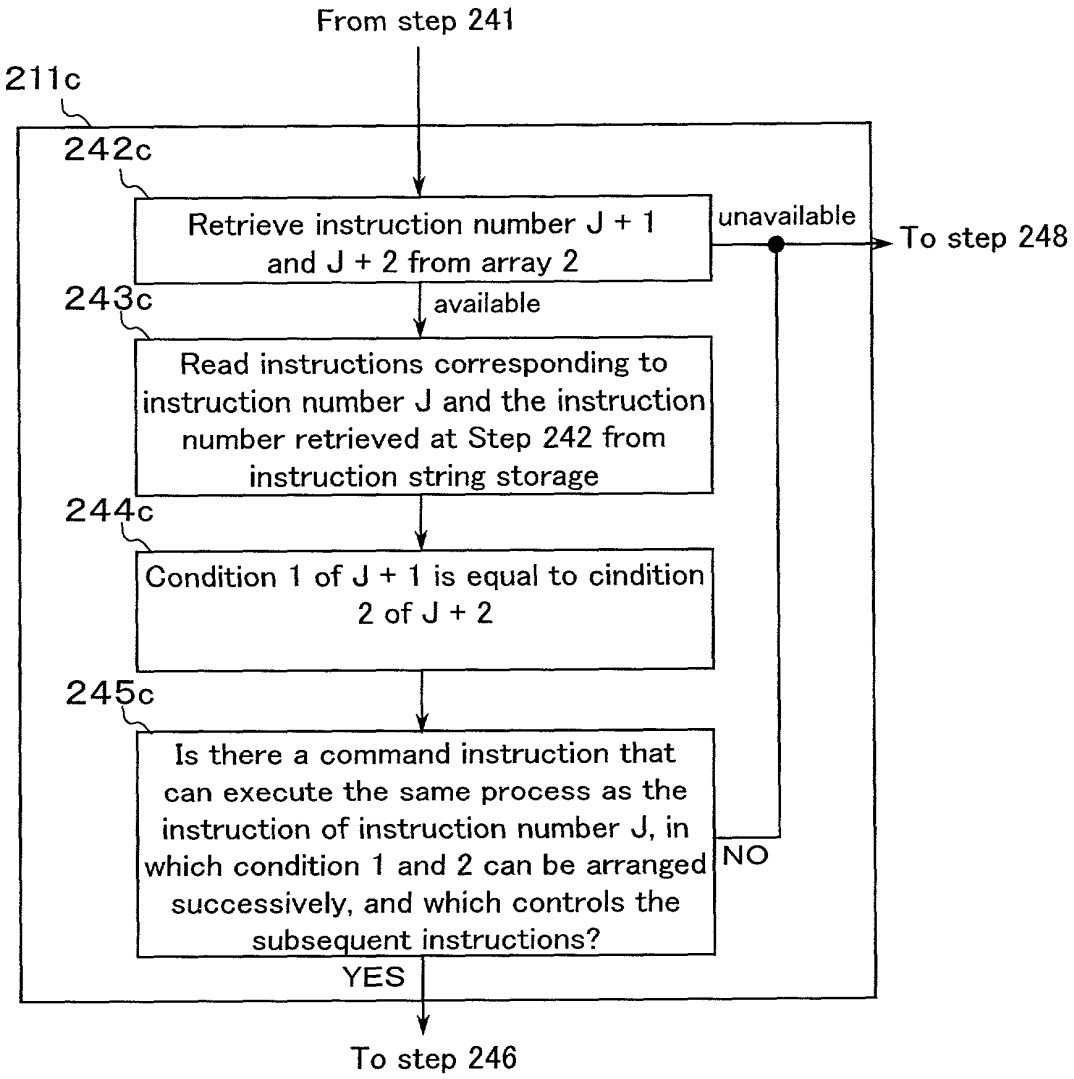
From step 241
211c
242c
Retrieve instruction number J + 1 and J + 2 from array 2
unavailable
To step 248
243c
available
Read instructions corresponding to instruction number J and the instruction number retrieved at Step 242 from instruction string storage
244c
Condition 1 of J + 1 is equal to cindition 2 of J + 2
245c
Is there a command instruction that can execute the same process as the instruction of instruction number J, in which condition 1 and 2 can be arranged successively, and which controls the subsequent instructions?
NO
YES
To step 246

FIG. 27

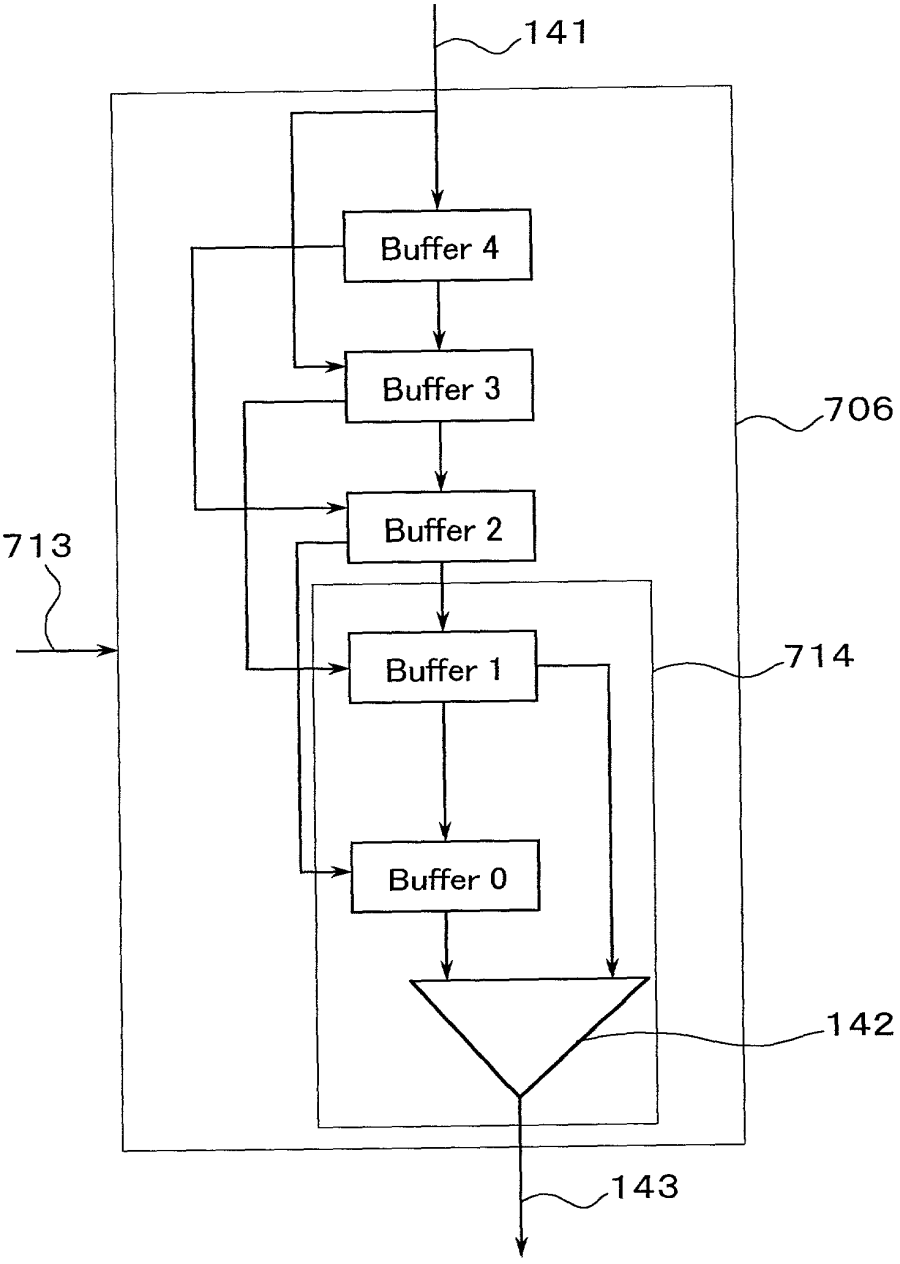
141
Buffer 4
Buffer 3
Buffer 2
Buffer 1
Buffer 0
706
713
714
142
143

FIG. 28

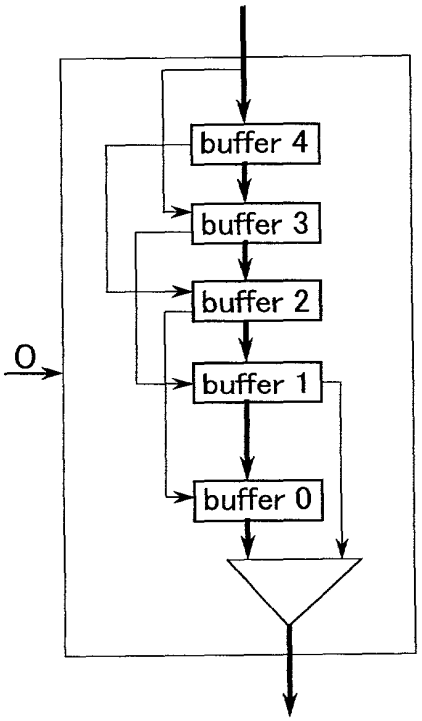

FIG. 29A

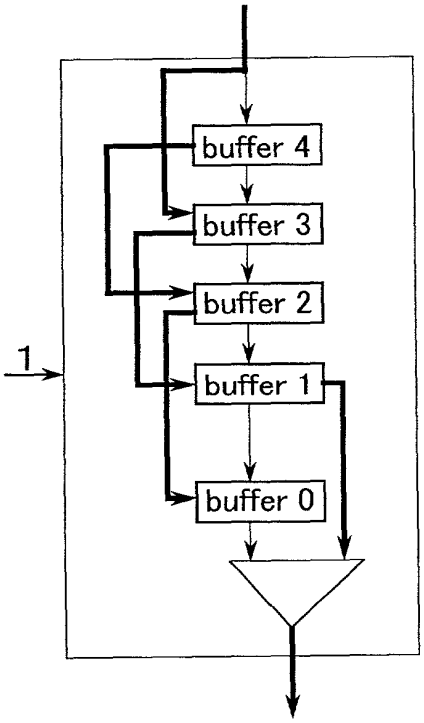

FIG. 29B

Conditional execution status / Exclusive condition	x'00	x'01	x'10	x'11
1	Instruction overriding signal "0"	×	Instruction overriding signal "0"	Instruction overriding signal "0"
0	Instruction overriding signal "0"	Instruction overriding signal "0"	Instruction overriding signal "1"	Instruction overriding signal "0"

FIG. 30A

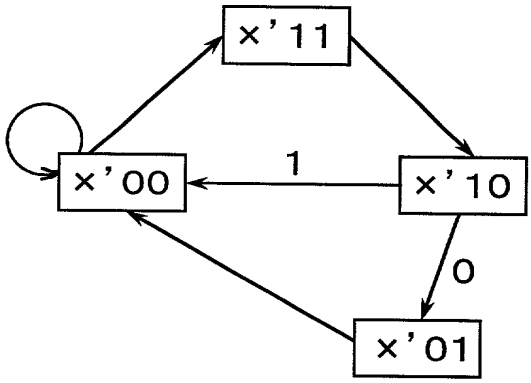

FIG. 30B

Conditional execution status / Exclusive condition	x'00	x'01	x'10	x'11
1	0	0	1	0
0	0	0	0	0

FIG. 30C

Buffer 4	Instruction 5	Instruction 6	Instruction 7	——	——
Buffer 3	Instruction 4	Instruction 5	Instruction 6	Instruction 8	Instruction 9
Buffer 2	Instruction 3	Instruction 4	Instruction 5	Instruction 7	Instruction 8
Buffer 1	Instruction 2	Instruction 3	Instruction 4	Instruction 6	Instruction 7
Buffer 0	Instruction 1	Instruction 2	Instruction 3	Instruction 5	Instruction 6

IF stage	Instruction 1	Instruction 2	Instruction 3	Instruction 5	Instruction 6
DEC stage		Instruction 1	Instruction 2	Instruction 4	Instruction 5
EX stage			Instruction 1	Instruction 2	Instruction 4

Conditional execution status	x'00	x'00	x'11	x'10	x'00	x'00
Instruction prefeth control signal	0	0	0	1	0	0
Exclusive condition	0	0	0	1	1	1
Instruction overriding signal	0	0	0	0	0	0
	t1	t2	t3	t4	t5	
	[t11 t12]	[t21 t22]	[t31 t32]	[t41 t42]	[t51 t52]	

FIG. 31

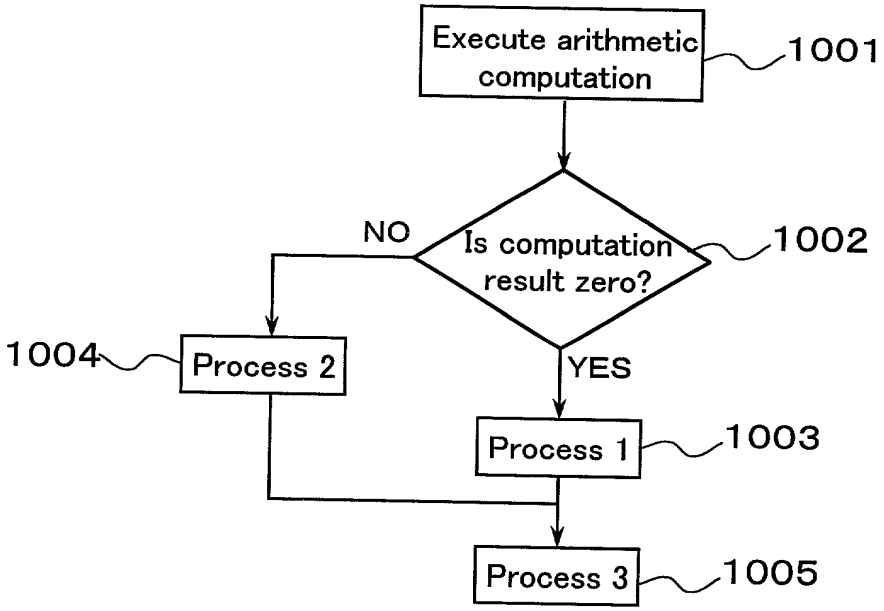

FIG. 32
(PRIOR ART)

First line	SUB R0,R1
Second line	BNE label 1
Third line	Instruction 1
Fourth line	JMP label 2
Fifth line	label 1: Instruction 2
Sixth line	label 2: Instruction 3

FIG. 33
(PRIOR ART)

First line	SUB R0,R1
Second line	MOVIFZF R2,R4
Third line	MOVIFNZF R3,R4
Fourth line	ADD R5,R6

FIG. 34
(PRIOR ART)

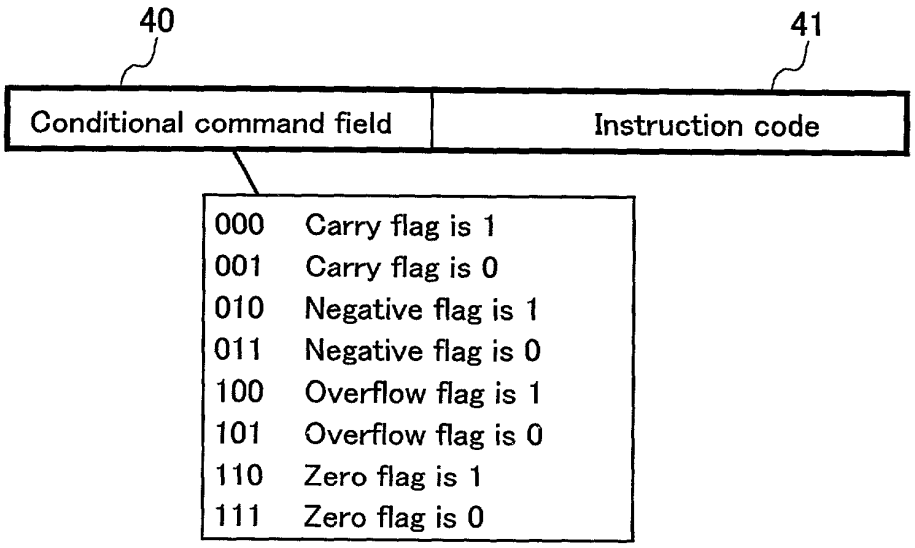

FIG. 35
(PRIOR ART)